DVCON U.S. 2021

March, 1 - 4 2021 | VIRTUAL

2021 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

CALL FOR EXTENDED ABSTRACTS

ORGANIZERS

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SUBMISSION PROCESS & DEADLINES

August 5, 2020
Submission Site Open

September 8, 2020
Abstract Submission Extended Deadline - **FINAL**

October 5, 2020
Official Accept/Reject Notification Sent to all Authors

October 12, 2020
Speaker Confirmation Forms Due

The Design & Verification Conference & Exhibition is the premier conference on the application of languages, tools, methodologies and standards for the design and verification of electronic systems and integrated circuits. The focus of this highly technical conference is on the practical aspects of these technologies and their use in leading-edge projects to encourage attendees to adopt similar techniques to improve their own design and verification flows. This year the conference will be completely virtual.

In addition to the specific topic areas suggested below, submissions may incorporate:

- Usage of Electronic Design Automation (EDA) tools such as simulation, emulation, formal verification, virtual prototyping and/or FPGA prototyping
- FPGA-based designs
- Usage of specialized design and verification languages such as SystemVerilog, SystemC, and e
- Assertions in SVA or PSL
- The use of general purpose and scripting languages such as C, C++, Perl, Python, Tcl and others
- Applications of the Accellera Portable Stimulus Standard
- Applications of design patterns or other innovative language techniques
- The use of AMS languages
- Internet of Things applications

Accepted authors will be invited and agree to do the following:

- Submit a draft paper between **October 26** and **November 15** for review
- Review and incorporate feedback from TPC, to be provided by **November 20**
- Submit a final paper and copyright form by **December 14**
- Submit a recorded oral or poster presentation for presentation at the virtual conference by **February 9**.

CONFERENCE SCHEDULE

Monday, March 1

- Accellera Day Tutorials
- Short Workshops
- Exhibits

Tuesday, March 2

- Technical sessions
- Keynote Speaker
- Exhibits

Wednesday, March 3

- Technical Sessions
- Panel Discussions
- Exhibits

Thursday, March 4

- Tutorials
- Workshops

Feel free to contact us for questions on the submission process at lleblanc@conferencecatalysts.com or visit DVCon.org.

CALL FOR EXTENDED ABSTRACTS Cont.

This call for abstracts solicits for papers and corresponding presentations that are highly technical and reflect real-life experiences and emerging trends in various domains. Submissions are encouraged in (but not restricted to) the following areas:

Topic Area 1: VERIFICATION & VALIDATION

- Advanced methodologies and testbenches
- Verification processes, regressions and resource management
- Debug and analysis of complex designs
- Multi-language design and verification
- Hardware/Software co-design and co-verification of embedded systems

Topic Area 2: SAFETY-CRITICAL DESIGN & VERIFICATION

- Verification and DO-254 compliance
- Automotive ISO 26262 Design and Verification Challenges
- Medical or Industrial Verification Challenges
- Requirements-Driven Verification Methodologies
- IP protection and security

Topic Area 3: MACHINE LEARNING AND BIG DATA

- Automating the Optimization of Verification Processes
- Coverage metrics and data analysis
- Performance modeling and/or analysis

Topic Area 4: DESIGN AND VERIFICATION REUSE & AUTOMATION

- Bridging verification and validation across multiple engines
- SoC and IP integration methods and tools
- Applications of the Accellera Portable Stimulus Standard
- Configuration management of IP and abstraction levels
- Interoperability of models and/or tools
- High-level synthesis from ESL languages
- Bridging virtual prototyping, simulation, emulation and/or FPGA prototyping

Topic Area 5: MIXED-SIGNAL DESIGN & VERIFICATION

- Mixed-signal design & verification techniques
- Real-value modeling approaches
- Application of mixed-signal extensions for UVM

Topic Area 6: LOW-POWER DESIGN & VERIFICATION

- Low-power design and verification
- Clock domain crossing verification
- Power modeling, estimation and management

DVCon honors the **Stu Sutherland Best Paper** and **Best Poster** submissions. The awards will be selected by the attendees at DVCon, based on the quality of both the paper and the presentation. **So please submit your abstract and join DVCon U.S. 2021!**

Please submit your extended abstract - **a minimum of 600 words, a maximum of 1,200 words (approximately 2 pages, not including diagrams, figures or tables)** - by **Monday, August 24th** to **epapers.org/dvcon2021** outlining your proposed presentation.

Full instructions and details for the extended abstract submission process can be found on DVCon.org.

EXTENDED ABSTRACT SUBMISSION GUIDELINES

The extended abstract should provide enough details so that the Technical Program Committee can evaluate the potential quality of your completed paper and the interest of the DVCon attendees in your presentation.

An extended abstract is expected to include the following details:

- Proposed paper title
- Name, affiliation, phone number, mailing address and email address for all authors.
- An introduction that specifies the context and motivation of the submission.
- A clear description of the specific contributions of your work.
- A summary that highlights results.
- Must use the suggested template format (found on the DVCon website).
- Must be a minimum of 600 words - maximum of 1200 words, approximately 2 pages.
- References, if appropriate.