DVCon US 2021 Panel Proposal

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Verification in the Open-Source Era

The idea of open source hardware, such as RISC-V that anyone can leverage to create their own CPU or custom accelerator, is tantalizing. Supporters believe freely available solutions will break open processor innovation and enable entry into new market segments. Blocks of open source IP already are implemented or in the process of being implemented in many of today's chip designs. Success seems assured.

Verification groups are hopeful but leery knowing verification is a much more complex problem than design. Most open source hardware is new and does not have the benefit of field-proven experience, which means verification groups are on the line to devise an untried verification flow, making a well-considered CPU verification strategy fundamental. Without those ingredients, it is impossible to have confidence in verification results.

Semiconductor Engineering's Brian Bailey will take a panel of design verification experts and open source proponents on an excursion into the open-source era to analyze the verification challenges. His questions will range from what compliance mean and how it is defined to whether it requires open source verification environments and what they would look like. By the panel's conclusion, panelists will have attempted to answer why verification is essential for success of the open source movement.

Moderator:
Brian Bailey
Technology Editor/EDA
Semiconductor Engineering

Panelists (no more than five):
Aldec
SmartDV
Imperas
Bluespec
Serge Leef/DARPA
Dennis Brophy/Mentor
Someone from OpenHW, Chips Alliance or RISC-V International