Accelerate signoff with JasperGold RTL Designer Apps

RTL designers are creating increasingly complex designs, and are under relentless pressure to provide assurance that the designs are complete, correct, and adhere to necessary coding rules, before handing off the designs for RTL verification and implementation. This assurance needs to be provided at the block/IP level as those become mature enough for handoff, and again once the design is integrated to subsystem or chip level. Recently, the multitude of asynchronous clock domains, driven by dynamic power optimization, and multiple reset domains have added further complexities. This has driven the need for clock and reset domain crossing checks (CDC/RDC) to be performed earlier as part of RTL signoff.

Traditional static verification techniques such as Lint, DFT, and structural CDC/RDC checkers have been unable to keep up with these growing complexities and have been unable to provide the level of assurance necessary for signing off today's designs. Designers are faced with structural checkers that often provide a huge list of potential violations, while lacking the intelligent automation support to help the designer process these violations. Hence the common designer complaint that these tools are "noisy".

In this workshop, we will take the attendees through using the JasperGold Superlint and CDC applications, which add formal verification technology and functional checks to these structural checks. The JasperGold technology supports the designers to identify the real problem violations, confirming fixes, and providing justification for waiving the violations that are not problematic. Additional automatic formal checks are provided for functional verification of many aspects of the design, using properties derived automatically from the RTL. Workshop attendees will learn how these JasperGold RTL Designer apps combine to "shift left" these checks, providing a much more complete level of automated verification. The result is that RTL designers are able to sign off higher quality, more robust and CDC/RDC-clean designs, months earlier in the project schedule.

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