DVCon US 2021 Workshop Proposal

Beyond Bug Hunting: Verification Coverage from Safety to Certification

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WORKSHOP CONTENT

Abstract

Understanding verification coverage is critical for meeting IC integrity standards and goes well beyond detecting bugs in the design. Without proper verification coverage metrics, meeting strict safety standards and certification may not be achievable. Precise metrics indicate where there are gaps in

verification and provide a clear view of the progress being made in the verification effort. Common simulation metrics are imprecise and only measure control coverage, resulting in significant lack in verification quality. These remedial practices are time-consuming and leave undetected bugs that could significantly impact design safety. Mutation analysis takes the risk out achieving safety signoff. Results and accurate and reproduceable, and this type of analysis creates reliable identification of verification gaps by highlighting over-constraining, dead and redundant code.

This workshop will explore how mutation analysis can have a positive impact on the safety of your design and provide the signoff confidence needed to achieve proper safety certification. In addition, the workshop will show how to achieve a meaningful integration of formal and simulation coverage metrics. A long-standing wish of many verification engineers and managers, coverage integration reduces effort overlap between simulation and formal and enables faster, more rigorous signoff.

Intended Audience

Managers; design and verification engineers developing digital hardware.

About Nicolae Tusinschi

Nicolae Tusinschi is Product Specialist Design Verification at OneSpin Solutions. Nicolae joined the team in 2016 as a quality assurance engineer and developed an exhaustive knowledge of OneSpin's complete suite of formal verification tools before targeting his attention on the company's OneSpin 360 DV™ design verification solution. His key projects have included integrating simulation coverage with formal results, leveraging coverage results in the verification process, and a case study on the application of formal verification to the I^2C serial protocol.

Nicolae holds a Bachelor of Science in Industrial Automation from "Dunărea de Jos" University of Galați (Romania) and a European Master's in Embedded Computing Systems (EMECS) awarded jointly by Technische Universität Kaiserslautern (Germany) and University of Southampton (United Kingdom). During his graduate studies, he completed his master's thesis, "Formal Verification of Proprietary Microcontroller IP," at Continental in Frankfurt, Germany.

Nicolae is based at OneSpin headquarters in Munich, Germany and is proficient in English, Romanian, Russian, and German.

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2020-10 V. 5