DVCon US 2021: Short Workshop

Affiliation: Agnisys

Presenter: Anupam Bakshi, Abhishek Bora

Topic: **RISC-V based SoC Design, Verification, and Validation in One Hour**

RISC-V brings a new wave to SoC development. Creating a fully validated design is an arduous process that takes several teams working together. Often the flow is a waterfall model where the specification is transformed in various stages of development. Sometimes aspects such as verification and validation are an afterthought. In order to speed up the process and get better quality of results, all aspects must be considered upfront.

We will talk about such an accelerated process in this workshop. Engineers will see a comprehensive example that will show them how to create an SoC based on RISC-V. We will deep-dive into the SoC design and complete it from start to finish.

Using a specification-centric methodology, we will take the attendees into a whirlwind one-hour flow of RISC-V based SoC design with semi-automatic verification and validation, all from a set of specifications.

Attendees will learn how to automate their development process such that there is zero redundancy and zero debug time. We will take a sample RISC-V design and create it in RTL, stitch it together with the CPU core and other IPs, verify it with UVM, and validate it in a bare-metal RISC-V based C-UVM environment. We will even touch on how to deal with interrupts, multiple masters and RISC-V custom instructions—all in the span of one hour!