Accellera Sponsored Short Workshop

UVM-SystemC and Randomization – Updates from the SystemC Verification Working Group

Speakers:

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- <tbd> (Members of Accellera VWG)

UVM-SystemC is an implementation of the Accellera UVM standard implemented in SystemC. Standardization efforts of UVM-SystemC is ongoing and multiple public review releases were released in the past years. Currently, the Accellera VWG is working on the standardization of a common randomization layer and a definition of functional coverage for UVM SystemC.

This workshop will introduce the basic concepts of UVM-SystemC and show how constrained randomization and functional coverage can be integrated to build a verification environment using the current UVM-SystemC library. Currently, the Accellera VWG is working on the standardization of a common randomization layer based on CRAVE, a C++, and SystemC constraint randomization library. The workshop will show how constrained randomization can be used within SystemC and integrated into UVM-SystemC verification environments.

In addition, the current standardization efforts within the Accellera Verification Working Group will be presented to show the progress and evolution of the UVM-SystemC standard.

The intended audience of this tutorial includes managers, system and verification engineers, and architects with basic knowledge in SystemC and/or UVM, which are interested in improving their system-level verification practices.