DVCon USA 2021
Short Workshop Abstract Submission

Sponsor	Circuitsutra Technologies Pvt Ltd
TITLE OF TUTORIAL	Fast forward your product launch using SHIFT LEFT: Hardware-Software co-design & co-verification using ESL methodologies
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ABSTRACT

Fast forward your product launch using SHIFT LEFT

Hardware-Software co-design & co-verification using ESL methodologies

The term 'Electronics System Level (ESL)' have been used in the industry for nearly two decades now. Different people use it in different context, with different meanings. It can be primarily generalized as the collection of methodologies that enables 'Hardware-Software Co-Design' and 'Raising the abstraction of chip design above RTL'.

The different technologies that are used to enable ESL methodologies are: C, C++, SystemC / TLM2.0 (IEEE 1666-2011), Python, UPF3.0 (IEEE1801-2015), IP-XACT (IEEE1685-2014), Portable Stimulus (new Accellera standard).

ESL methodologies are not supposed to replace the traditional RTL-GDS flow, but rather co-exist with existing flow and augment it to perform various advanced activities which are not feasible with traditional flow. It enables Pre-Silicon firmware development, Architecture exploration to optimize power & performance early in the cycle at system level, High-Level Synthesis (HLS), SoC Level simulation, System level simulation, Hardware-Software co-design and co-verification.

In this workshop we will briefly touch upon various use cases of ESL methodologies and discuss the best practices being used in the industry.

There are two interesting phenomenon happening in the semiconductor industry today, and these are driving the numerous numbers of new SoC designs being kicked off:

1. SoC architectures for Artificial Intelligence / Deep Learning
2. Open source hardware movement

Artificial Intelligence / Deep Learning SoC are required to perform very specific tasks: Massively parallel & heterogenous matrix multiplication, Accelleration of neural network etc.. and requires real time data connectivity. The SoC to be used in edge devices have further unique requirements – extremely low power consumption, small form factors etc.. Lots of innovation is happening in the industry for designing new kind of SoC architectures. ESL methodologies can be effectively deployed in the design & verification of these SoC and the systems using these SoC

Open source hardware movement is primarily fuelled by RISC-V, which is a open source Instruction Set Architecture (ISA), and supports adding new custom instructions. Further there are industry consortium like Chips Alliance and OpenHW group that are driving the open source implementation of processor cores, Peripherals, Bus protocols and complete SoC.

We will discuss about the SystemC based ESL methodologies for this RISC-V based open soure ecosystem.