System-level Power Analysis with IEEE 2416 Power Models

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Abstract:
Opportunities for reducing power at the system level are understood to be significant, but system level low power design automation has lagged in large part due to the lack of standardized, inter-operable, power models. This lack of models motivated the development of IEEE 2416 (also known as Unified Power Models, or UPM). This workshop will describe this new modeling technology, the novel tools and methodologies it enables, and the inter-operation of 2416 power data models with IEEE 1801 power state models.

IEEE 2416 addresses the power modeling needs of three distinct groups of users: IP providers and model producers, system architects and verification teams, and EDA developers. IP providers benefit from 2416's ability to represent Process-Voltage-Temperature (PVT) independent models, greatly reducing the model generation resources needed to build and validate power data models. The ability to analyze system level power, using models in an industry standard format, is of great value to System Architects while System Validation teams can easily verify power consumption, taking advantage of 1801's and 2416's standardized interoperation. And 2416's ability to enable the late binding of PVT conditions and represent both system and gate level blocks will provide EDA developers opportunities to create new power aware tools and methodologies.

2416's rich semantics facilitate easy and interoperable model exchange by providing four different data representations (scalars, tables, expressions, contributors) and three different modeling levels (system, gate or bit level, multi-level). Creation of bottom-up

models, based on design data and power contributors (PVT independent power proxies) and top-down models, based on measured or simulated data, will be described in detail for common IP blocks, such as a memory and a RISC-V processor. The memory model will illustrate how design data from one process technology can be easily and accurately mapped to a different technology. The RISC-V will be modeled with an Energy per Instruction (EPI) format in which each instruction is characterized individually and represented for both cache hit and miss conditions, making the model's power consumption sensitive to the details of the code stream it is running.

This workshop is for designer engineers and verification engineers of power and temperature constrained systems and related design automation. Attendees will learn how to develop UPM/2416 power data models and use them with UPF/1801 power state models and emerging system level power analysis tools.

Presenter bios:

Nagu Dhanwada, IBM

Nagu Dhanwada is a Senior Technical Staff Member in IBM Systems group, who leads the development of power, reliability, thermal tools and methodologies. He has a PhD in Computer Engineering from University of Cincinnati. He is the chair of the Si2 Low Power Coalition, and the IEEE P2416 power modeling standards committee. He has a corporate award, was named best of IBM in 2015 and has several patents and publications in the areas of low power design, analysis, optimization, modeling, analog design and electronic system level design.

Rhett Davis, NCSU

W. Rhett Davis is a Professor of Electrical and Computer Engineering at North Carolina State University. He received B.S. degrees in electrical and computer engineering from North Carolina State University, Raleigh, in 1994 and M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley in 1997 and 2002. He received the National Science Foundation's Faculty Early Career Development (CAREER) award in 2007. He received the Distinguished Service Award from the Silicon Integration Initiative (Si2) in 2012 for his research in the development of standards for electronic design automation (EDA) and his development of the *FreePDK* open-source, predictive process design kit. He works currently with Si2 to develop standards for system-level power-modeling and compact modeling of device reliability. He has been an IEEE member since 1993 and became a Senior Member in 2011. He has published over 50 scholarly journal and conference articles. He has worked briefly at Hewlett-Packard (now Keysight) in Boeblingen, Germany and consulted for Chameleon Systems, Qualcomm, BEECube, and Silicon Cloud International.

Dr. Davis' research is centered on electronic design automation for integrated systems in emerging technologies. He is best known for his efforts in design enablement, 3DIC design, thermal analysis, circuit simulation, and power modeling for systems-on-chip and chip multi-processors.

Jerry Frenkil, Si2

Jerry Frenkil is the Director of OpenStandards for Si2. He has over 30 years of experience in the semiconductor and EDA industries as a designer, technologist, entrepreneur, and executive and currently serves as vice-chair of the IEEE P2416 Working Group on System Level Power Modeling. Jerry co-founded Sente, which later became Sequence Design where he was CTO and VP of R&D. He has also worked as an independent design consultant and has held management positions at Nanowatt Design, VLSI Technology and Mostek. Jerry holds a BSEE from the University of Texas, has published over twenty articles including four book chapters on Low Power Design, and holds a dozen patents in circuit design and design automation.

David Ratchkov, Thrace Systems

David has spent 20 years in the semiconductor industry working on all aspects of Power, with most recent focus on modeling, estimation and analysis, optimization and correlation. His career started at LSI Logic and has most recently worked at Broadcom's Storage Group, before starting his own company Thrace Systems, focused on EDA Tools on Power analysis.