DVCon US 2021 Short Workshop Proposal

Title
Functional SoC and Early Firmware Verification Using a Virtual Realization Layer

Abstract (50-100 words)
SoC Verification has become more important in recent years. However, this task is challenging given the increased complexity of UVM for larger systems, emulation usage and the need to drive processors as part of the system. This tutorial will provide a methodology using a virtual realization layer, as suggested by the PSS committee, which can perform various OS-like capabilities while streamlining hardware verification tool usage. It may also be used to aid firmware verification with the hardware.

Description
Functional verification at the system or sub-system level is becoming more common, and necessary given that SoC functionality is spread over multiple IP blocks and software. However, creating test content for these verification projects is challenging, particularly given the increased complexity of UVM usage in larger systems, the use of emulation and prototyping, and the need to drive processor subsystems with OS-style capabilities, such as memory allocation.

Providing a layer in between the test content and the SoC model that handles housekeeping requirements, plus also streamlining the methodology of hardware verification engines and enabling portability from UVM IP tests and for post silicon is extremely useful. Indeed, the Accellera Portable Stimulus Committee have included some basic language features in the latest 2.0 version of the Portable Stimulus Standard to drive such a layer.

Furthermore, such a solution may also benefit the firmware team by allowing them to leverage a realistic model earlier in the development process. It may also allow firmware prototypes to be run on earlier hardware models, improving coverage and testing the overall specification between the teams.

This tutorial will focus on the use of virtual realization, explain how this layer may be implemented relatively easily, how it may be applied to both SoC and UVM block verification, and how it can increase the shift-left opportunities in a project, while accelerating hardware verification methodologies. We will show how it may be used with the new PSS 2.0 standard, as well as leveraged in UVM testbenches and C-code SoC test environments.

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A second presenter from a large semiconductor company who has used this technology. We are still working with them to see if this is possible.