Title: Early Design and Validation of an AI Accelerator's System Level Performance Using an HLS Design Methodology

Format: Lecture

Author: Michael Fingeroff
Bio: Michael Fingeroff has worked as an HLS Technologist for the Catapult High-Level Synthesis Platform at Mentor, A Siemens Business since 2002. His areas of interest include Machine Learning, DSP, and high-performance video hardware. Prior to working for Mentor, he worked as a hardware design engineer developing real-time broadband video systems. Mike Fingeroff received both his bachelor's and master's degrees in electrical engineering from Temple University in 1990 and 1995 respectively.

Abstract:
One of the fastest growing areas of hardware and software design is Artificial Intelligence (AI)/Machine Learning (ML), fueled by the demand for more autonomous systems like self-driving vehicles and voice recognition for personal assistants. Many of these algorithms rely on Convolutional Neural networks (CNNs) to implement deep learning systems. While the concept of convolution is relatively straightforward, the application of CNNs to the ML domain has yielded dozens of different neural network architectures. While these networks can be executed in software on CPUs/GPUs, the power requirements for these solutions make them impractical for most inferencing applications, the majority of which involve portable, low-power devices.

This workshop will show how a High-Level Synthesis (HLS) design and verification flow built around Catapult, and the ecosystem around it, could dramatically speed up the design of the AI/ML hardware accelerators compared to a traditional RTL based flow. It will focus on using the open-source MatchLib SystemC library from NVIDIA to perform rapid modelling and synthesis of the ML accelerator. The workshop will demonstrate how pre-hls simulation using MatchLib can identify and fix potential system-level performance issues that are normally not found till very late in a hand-coded RTL design methodology. Finally we will present 2-3 customer case-studies showcasing how these technologies work in conjunction to address our customers HLS design and verification challenges.