

Title: Workshop from Accellera UVM-AMS Standard Working Group

Abstract:

Based on various discussions with user companies, it was established that there was a strong interest in the standardization of UVM-AMS. An Accellera Proposed Working Group (PWG) and then a Working Group (WG) were formed, based on Accellera Board of Directors' recommendation, with a charter to develop a standard that will provide a unified analog/mixed-signal verification methodology based on UVM, with major focus on transient analysis.

The UVM-AMS standard will provide a comprehensive and unified analog/mixed-signal verification methodology based on UVM to improve analog mixed signal (AMS) and digital mixed signal (DMS) verification of integrated circuits and systems. This will encourage support by tool and IP providers, offering ready-to-use analog/mixed-signal verification IP that can be integrated easily into a UVM-AMS testbench. It will raise the productivity and quality of analog/mixed-signal verification across projects and applications, thanks to the reuse of proven verification components, and stimuli.

In this workshop, the WG would share the findings, requirements and ideas collected so far and the next step plan for the standardization and would like to receive feedback from the analog/mixed-signal verification community.

The following main aspects of the UVM-AMS standard under consideration will be discussed at high level in this Workshop.

- 1) A UVM-ASM framework for the creation of analog/mixed-signal verification components and test benches by introducing both extensions to digital centric UVM verification IP classes and also related module-based components to facilitate interactions between the class-based and structural environments.
- 2) A set of class-based extensions to UVM related to driver, monitor, scoreboard, etc., to support analog/mixed-signal verification
- 3) A set of components and/or packages in SystemVerilog and/or Verilog-AMS to facilitate interactions between the class-based and structural environments and to interface with various types of Analog Design Representations.
- 4) A set of Application Programming Interfaces (APIs) to enable the development of modular, scalable, and reusable verification components and test benches, including stimulus, sequence and analysis functions, etc.
- 5) A framework for creation of Mixed Signal Verification UVM verification components (UVCs) or extensions of existing UVCs for enhanced stimulus, analysis, monitoring and debug capabilities.

In addition, the requirements collected so far for the following elements will be presented and discussed as well.

- 1) Driver,
- 2) Monitor,

- 3) Sequencer,
- 4) Checker,
- 5) Types of Data and Signal Abstractions (electrical, real, ...),
- 6) Randomization,
- 7) Different Types of Design Representation (SPICE Netlist, Verilog-AMS, Real Number Modeling)
- 8) Analog Signal Characteristics and Its Generation (RF style, Noise, Jitter, ...)
- 9) Coverage,
- 10) Assertion and Assumptions.
- 11) Basic Libraries and/or packages of tunable checker classes, assertions, transfer functions, time-to-frequency domain transformations, and so on.

Finally, an example will be illustrated about how a UVM_AMS VIP (or UVC) Package looks like, and how the user would be able to integrate and use it in a smooth and efficient way.

At the end, we would like to hear from the audience with comments, questions, and suggestions.