DVCon US 2021 "Short Workshop" submission:

Multi Language Verification Framework Standardization and Demo

The Accellera Multi Language Verification Working Group (MLVWG) is currently developing a proof-of-concept (PoC) implementation and demonstrator for creating a standards-based approach for combining verification environments developed in different languages. The aim of this multi-language verification framework is to enable interoperability and reuse of verification environments and components across the language boundary. The objective of the Multi Language Verification WG is to standardize the API along with a reference implementation, to facilitate industry adoption and deployment of multi-language verification technologies and methodologies.

In this short workshop, the MLVWG presents the current status of the proof-of-concept implementation and demonstrate its capabilities. A multi-language example is presented, which combines the Universal Verification Methodology (UVM) library in SystemVerilog and SystemC. Based on this example, the multi-language verification framework, its foundation concepts and the API targeted for standardization is explained and discussed.

In addition, multi-language-specific UVM standardization requirements will be presented and language extensions are proposed to address seamless integration and interoperability between UVM verification frameworks in SystemVerilog and SystemC.

Presenters:

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