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Presenter Biography

Mihajlo Katona is an experienced semiconductor industry engineer with 20+ years of design and verification experience. In the past few years, he was focused on VLSI projects with supporting functional verification work for power management ICs, computer vision processing unit with machine learning hardware accelerators, IoT processors, hardware engines for LTE-5G supporting tasks, DSP memory subsystems, and multicore DSP for multigigabit low latency applications. Mihajlo holds a Ph.D. degree in computer engineering from the University of Novi Sad, Serbia.

Workshop Title – *Verification of Functional Safety for an Automotive AI Processor*

Presentation Abstract –

Modern integrated circuits meet new data safety challenges. This functionality is primarily required by the auto and aviation industry where any integrated circuit used in the vehicle must comply with rigorous standards in terms of data preservation. In unforeseen situations, such as operations outside the declared temperature range or in the presence of strong electromagnetic waves, circuitry must maintain data consistency by applying specific safety mechanisms.

This presentation is addressing the handling of random failures during the design and verification of the CEVA IPs designed to be parts of a complex automotive system. By analyzing architectural aspects of modern integrated circuits we will identify critical design features and we will review principles for verification of safety mechanisms based on an example of an AI processor for on-chip deep learning inferencing, computer vision tasks, and fusing data from multiple sensors such as radar, lidar, time-of-flight, microphones, and other inertial measurement units.

We will present insights into the constrained-random verification methodology for verifying circuitry with safety mechanisms. The methodology is based on error injection bus functional models and includes a set of verification components verifying different safety features such as memory protection, bus protection, register protection, latent testing, and online BIST safety checkers. Error injection mechanisms will present principles for verifying ECC logic and CRC circuitry. In-system testing for lifetime reliability will be covered with the presentation of latent testing methodology. In the presentation, we will address the automotive standard ISO 26262, but the focus will be on engineering solutions and technical approach for protecting data movements in the circuitry with safety mechanisms in place.

Further, in this workshop, we will present the concept of a continuous review process for assuring requirement traceability we have applied as part of overall product safety analysis. The safety targets are defined with a set of requirements that must be tested at each verification level according to the V-model as per related safety standards. The presentation will illustrate examples of all review steps converging towards sign-off review and link them to the verification pyramid showing randomization levels at different verification layers.